

A-821PG

Hardware User's Manual

Warranty

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1. Introduction

1.1 General Description

The A-821PGL/PGH is a high performance, multifunction analog, digital I/O board for the PC AT compatible computer. The A-821PGL provides low gain (1, 2, 4, 8). The A-821PGH provides high gain (1,10,100,1000). The A-821PGL/PGH contains a 12-bit ADC with up to 16 single-ended or 8 differential analog inputs. The maximum sample rate of the A/D converter is about 45 k sample/sec. Also included is a 12-bit DAC for voltage output, and 16 channels of TTL-compatible digital input, 16 channels of TTL-compatible digital output.

The NDA version of the A-821PGL provides 16 single-ended analog input or 8 channels of differential analog input. The A-821PGL NDA version doesn't provides analog output and digital I/O function.

1.2 Features

- The maximum sample rate of the A/D converter is about 45 k sample/sec.
- Software selectable input ranges
- PC AT compatible ISA bus
- A/D trigger mode : software trigger , pacer trigger
- 16 single-ended or 8 differential analog input signals
- Programmable high gain : 1,10,100,1000 (A-821PGH)
Input range : $\pm 5\text{ V}, \pm 0.5\text{ V}, \pm 0.05\text{ V}, \pm 0.005\text{ V}$
- Programmable low gain : 1,2,4,8 (A-821PGL)
Input range : $\pm 5\text{ V}, \pm 2.5\text{ V}, \pm 1.25\text{ V}, \pm 0.625\text{ V}$
- 1 channel 12-bit D/A voltage output (A-821PGL/PGH only)
- 16 digital input /16 digital output (TTL compatible) (A-821PGL/PGH only)
- Interrupt handling

1.3 Specifications

A-821PGL / PGH provides Analog input, Analog output and Digital I/O functions

A-821PGL/NDA version provides analog input function only

Model Name	A-821PGH/PGL
Analog Input	
Channels	16 single-ended / 8 differential
A/D Converter	12-bit, 8 μ s conversion time
Sampling Rate	45 kS/s. max.
Over voltage Protection	Continuous +/-35 Vp-p
Input Impedance	10 M Ω /6 pF
Trigger Modes	Software, Pacer
Data Transfer	Polling, Interrupt
Accuracy	0.01 % of FSR \pm 1 LSB @ 25 $^{\circ}$ C, \pm 10 V
Zero Drift	15 ppm/ $^{\circ}$ C of FSR
Analog Output	
Channels	1 independent
Resolution	12-bit
Accuracy	0.01 % of FSR \pm 1 LSB @ 25 $^{\circ}$ C, \pm 10 V
Output Range	Unipolar: 0 ~ 5 V, 0 ~10 V / Bipolar: +/-10 V
Output Driving	+/- 5 mA
Slew Rate	0.6 V/ μ s
Output Impedance	0.1 Ω max.
Operating Mode	Software
Digital Input	
Channels	16
Compatibility	5 V/TTL
Input Voltage	Logic 0: 0.8 V max. / Logic 1: 2.0 V min.
Response Speed	1.0 MHz (Typical)
Digital Output	
Channels	16
Compatibility	5 V/TTL
Output Voltage	Logic 0: 0.4 V max. / Logic 1: 2.4 V min.
Output Capability	Sink: 0.8 mA @ 0.8 V / Source: -2.4 mA @ 2.0 V
Response Speed	1.0 MHz (Typical)
Timer/Counter	
Channels	3 independent
Resolution	16-bit
Compatibility	5 V/TTL
Input Frequency	10 MHz max.
Reference Clock	Internal: 2 MHz
General	
Bus Type	ISA
I/O Connector	Female DB37 x 1 / 20-pin box header x 2
Dimensions (L x W x D)	160 mm x 106 mm x 22 mm
Power Consumption	300 mA @ +5 V 60 mA @ +12 V 30 mA @ -12 V
Operating Temperature	0 ~ 60 $^{\circ}$ C
Storage Temperature	-20 ~ 70 $^{\circ}$ C
Humidity	5 ~ 85% RH, non-condensing

- Analog Input Range : (software programmable)

Model	A-821PGL (Low-Gain)				
Gain	0.5	1	2	4	8
Bipolar (V)	+/- 10	+/- 5	+/- 2.5	+/- 1.25	+/- 0.625
Sampling Rate Max.	45 kS/s				
Model	A-821PGH (High-Gain)				
Gain	0.5	1	10	100	1000
Bipolar (V)	+/- 10	+/- 5	+/- 0.5	+/- 0.05	+/- 0.005
Sampling Rate Max.	45 kS/s		10 kS/s		1 kS/s

Note:A-821PGL/NDA version without this function

1.3.1 Applications

- Signal analysis
- FFT & frequency analysis
- Transient analysis
- Production test
- Process control
- Vibration analysis
- Energy management
- Industrial and lab. measurement and control

1.4 Product Check List

The package includes the following items:

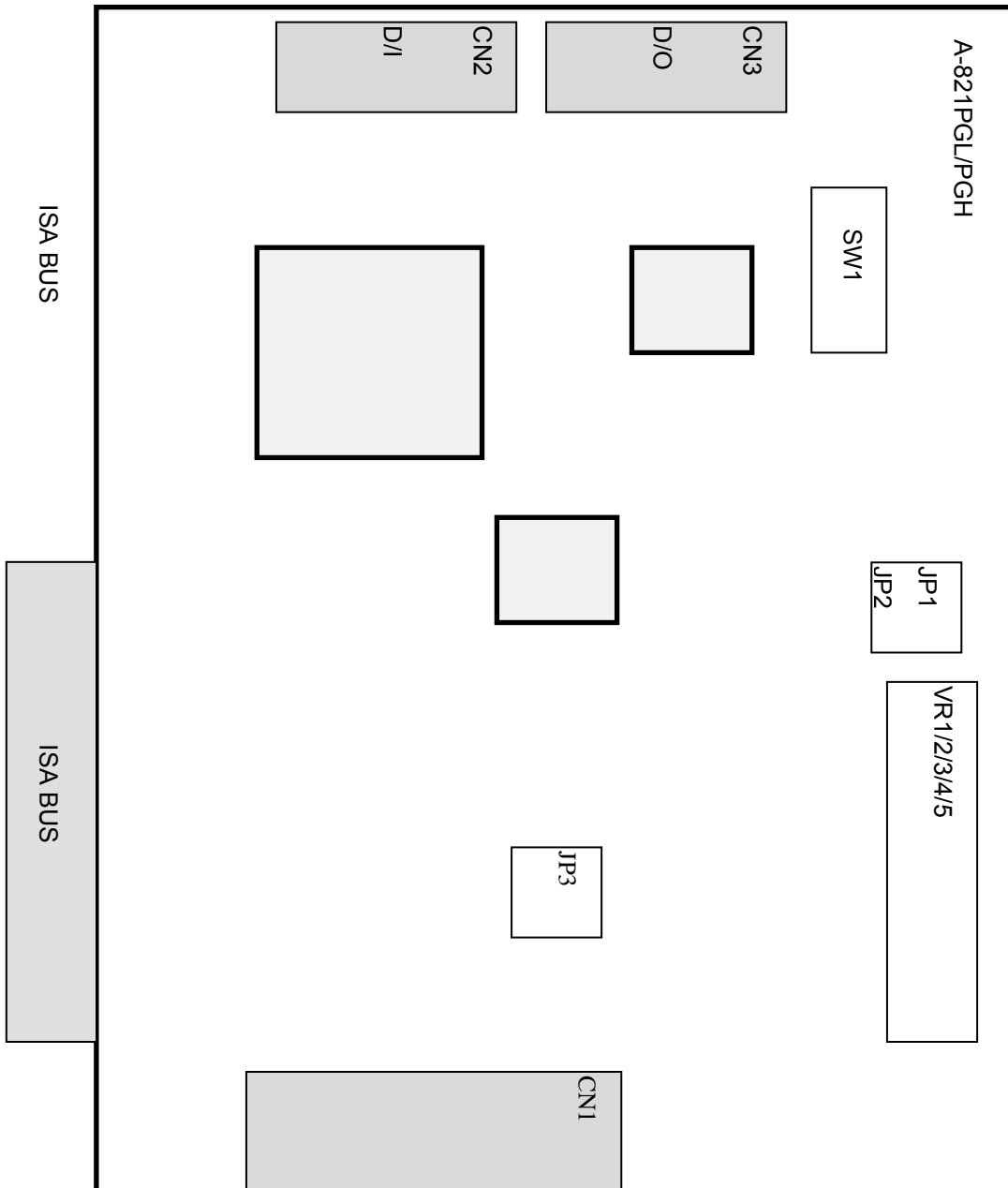
- One piece of A-821PGL/PGH multifunction card
- One company CD
- One Quick Start Guide

Attention !

If any of these items are missing or damaged, contact the dealer who provided you with this product. Save the shipping materials and carton in case you want to ship or store the product in the future.

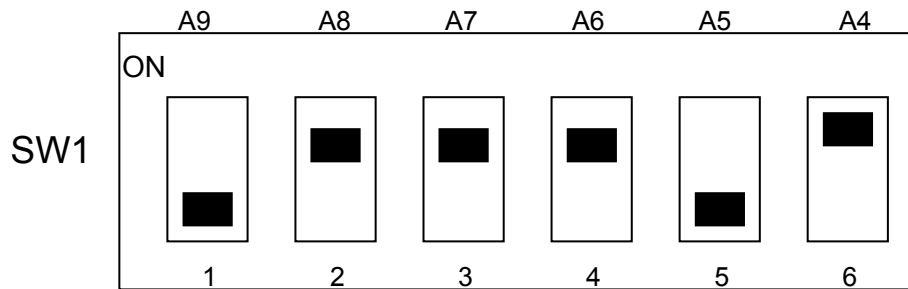
2. Hardware Configuration

2.1 Board Layout



2.2 I/O Base Address Setting

The A-821PGL/PGH occupies 16 consecutive locations in I/O address space. The base address is set by DIP switch SW1. The default address is 0x220.



Default Base Address 220 Hex

For Example

How to select 2 2 0 (Hex)

OFF → 1
ON → 0

	2		2				0
	OFF	ON	ON	ON	OFF	ON	
→	1	0	0	0	1	0	
	A9	A8	A7	A6	A5	A4	

The detail SW1 base addresses setting. Please refer to **2.2.1 Base Address Table**.

2.2.1 Base Address Table

(*): Default base address

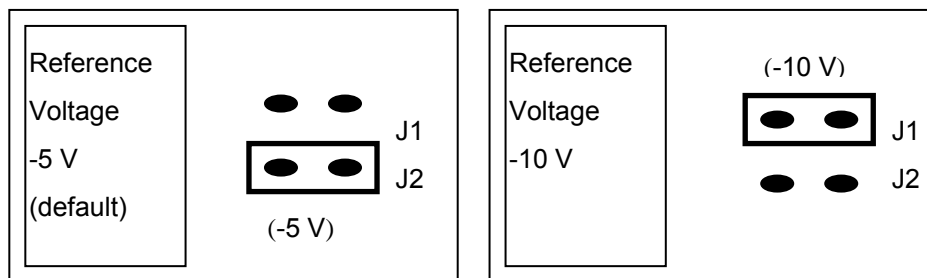
Base Addrs	1 A9	2 A8	3 A7	4 A6	5 A5	6 A4
200-20F	OFF	ON	ON	ON	ON	ON
210-21F	OFF	ON	ON	ON	ON	OFF
220-22F (*)	OFF	ON	ON	ON	OFF	ON
230-23F	OFF	ON	ON	ON	OFF	OFF
240-24F	OFF	ON	ON	OFF	ON	ON
250-25F	OFF	ON	ON	OFF	ON	OFF
260-26F	OFF	ON	ON	OFF	OFF	ON
270-27F	OFF	ON	ON	OFF	OFF	OFF
280-28F	OFF	ON	OFF	ON	ON	ON
290-29F	OFF	ON	OFF	ON	ON	OFF
2A0-2AF	OFF	ON	OFF	ON	OFF	ON
2B0-2BF	OFF	ON	OFF	ON	OFF	OFF
2C0-2CF	OFF	ON	OFF	OFF	ON	ON
2D0-2DF	OFF	ON	OFF	OFF	ON	OFF
2E0-2EF	OFF	ON	OFF	OFF	OFF	ON
2F0-2FF	OFF	ON	OFF	OFF	OFF	OFF
300-30F	OFF	OFF	ON	ON	ON	ON
310-31F	OFF	OFF	ON	ON	ON	OFF
320-32F	OFF	OFF	ON	ON	OFF	ON
330-33F	OFF	OFF	ON	ON	OFF	OFF
340-34F	OFF	OFF	ON	OFF	ON	ON
350-35F	OFF	OFF	ON	OFF	ON	OFF
360-36F	OFF	OFF	ON	OFF	OFF	ON
370-37F	OFF	OFF	ON	OFF	OFF	OFF
380-38F	OFF	OFF	OFF	ON	ON	ON
390-39F	OFF	OFF	OFF	ON	ON	OFF
3A0-3AF	OFF	OFF	OFF	ON	OFF	ON
3B0-3BF	OFF	OFF	OFF	ON	OFF	OFF
3C0-3CF	OFF	OFF	OFF	OFF	ON	ON
3D0-3DF	OFF	OFF	OFF	OFF	ON	OFF
3E0-3EF	OFF	OFF	OFF	OFF	OFF	ON
3F0-3FF	OFF	OFF	OFF	OFF	OFF	OFF

The PC I/O port mapping is given below.

ADDRESS	Device	ADDRESS	Device
000-1FF	PC reserved	320-32F	XT Hard Disk
200-20F	Game/control	378-37F	Parallel Printer
210-21F	XT Expansion Unit	380-38F	SDLC
238-23F	Bus Mouse/Alt. Bus Mouse	3A0-3AF	SDLC
278-27F	Parallel Printer	3B0-3BF	MDA/Parallel Printer
2B0-2DF	EGA	3C0-3CF	EGA
2E0-2E7	AT GPIB	3D0-3DF	CGA
2E8-2EF	Serial Port	3E8-3EF	Serial Port
2F8-2FF	Serial Port	3F0-3F7	Floppy Disk
300-31F	Prototype Card	3F8-3FF	Serial Port

2.3 Jumper Setting

2.3.1 JP1 : D/A Internal Reference Voltage Selection

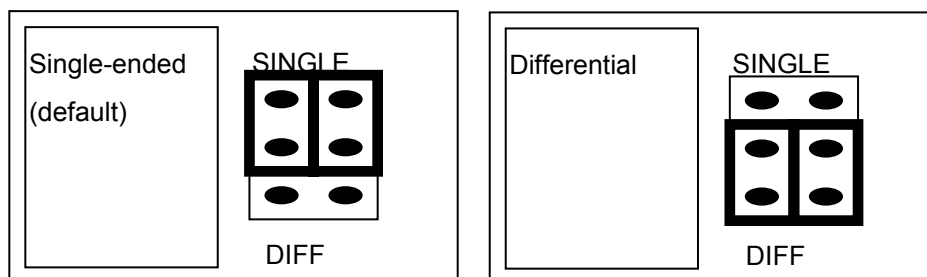


Select (-5 V) : D/A voltage output = 0 ~ 5 V (both channel)

Select (-10 V): D/A voltage output = 0 ~ 10 V (both channel)

JP1 is valid only if JP2 selects D/A internal reference voltage

2.3.2 JP3 : Single-ended/Differential Selection



The A-821PGL/PGH offers 16 single-ended or 8 differential analog input signals.

The JP3 selects single-ended/differential. The user can not select single-ended and differential simultaneously.

Refer to Sec. 2.9 first.

2.4 I/O Register Address

The A-821PGL/PGH occupies 16 consecutive PC I/O addresses.

The following table lists the registers and their locations.

Address	Read	Write
Base+0	Reserved	Reserved
Base+1	8254 Counter 1	8254 Counter 1
Base+2	8254 Counter 2	8254 Counter 2
Base+3	Reserved	8254 Counter Control
Base+4	A/D Low Byte	D/A Channel 0 Low Byte
Base+5	A/D High Byte	D/A Channel 0 High Byte
Base+6	DI Low Byte	Reserved
Base+7	DI High Byte	Reserved
Base+8	Reserved	A/D Clear Interrupt Request
Base+9	Reserved	A/D Gain Control
Base+A	Reserved	A/D Multiplexer Control
Base+B	Reserved	A/D Mode Control
Base+C	Reserved	A/D Software Trigger Control
Base+D	Reserved	DO Low Byte
Base+E	Reserved	DO High Byte
Base+F	Reserved	Reserved

2.4.1 8254 Counter

The 8254 Programmable timer/counter has 4 registers from Base+0 through Base+3. For detailed programming information about the 8254, please refer to Intel's "Microsystem Components Handbook".

Address	Read	Write
Base+1	8254 Counter 1	8254 Counter 1
Base+2	8254 Counter 2	8254 Counter 2
Base+3	Reserved	8254 Counter Control

2.4.2 A/D Input Buffer Register

(READ) Base+4 : A/D Low Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

(READ) Base+5 : A/D High Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	BUSY	D11	D10	D9	D8

A/D 12 bits data : D11...D0, D11=MSB, D0=LSB

BUSY =1 : A/D 12 bits of data busy

=0 : A/D 12 bits of data ready

The low 8 bits of A/D data are stored in address BASE+4 and the high 4 bits of data are stored in address BASE+5. The BUSY bit is used as an indicator for A/D conversion. **When an A/D conversion is completed, the BUSY bit will be cleared to zero.**

2.4.3 D/A Output Latch Register

(WRITE) Base+4 : Channel 1 D/A Low Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

(WRITE) Base+5 : Channel 1 D/A High Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	D11	D10	D9	D8

D/A 12 bits of output data : D11..D0, D11=MSB, D0=LSB, X=don't care

The D/A converter will convert the 12 bits of digital data to analog output. The low 8 bits of **D/A channel** are stored in address BASE+4 and high 4 bits are stored in address BASE+5. The D/A output latch registers are designed as a “**double buffered**” structure, so the analog output latch registers will be updated until the high 4 bits of digital data are written. **the user must send low 8 bits first and then send high 4 bits to update the 12 bits AD output** latch register.

NOTE : Send low 8 bits first, then send high 4 bits.

2.4.4 D/I Input Buffer Register

(READ) Base+6 : D/I Input Buffer Low Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

(READ) Base+7 : D/I Input Buffer High Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D15	D14	D13	D12	D11	D10	D9	D8

D/I 16 bits of input data : D15..D0, D15=MSB, D0=LSB

The A-821PGL/PGH provides 16 TTL compatible digital inputs. The low 8 bits are stored in address BASE+6. The high 8 bits are stored in address BASE+7.

2.4.5 Clear Interrupt Request

(WRITE) Base+8 : Clear Interrupt Request Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	X	X	X

X=don't care, XXXXXXXX=any 8 bits of data are valid

If the A-821PGL/PGH is working in the interrupt transfer mode, an on-board hardware status bit will be set after each A/D conversion. This bit must be **cleared by software** before the next hardware interrupt. Writing any value to address BASE+8 will clear this hardware bit and the hardware will generate another interrupt when the next A/D conversion is completed.

2.4.6 A/D Gain Control Register

(WRITE) Base+9 : A/D Gain Control Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	X	GAIN1	GAIN0

The Only difference between the A-821PGL and the A-821PGH is the **GAIN** control function. The **A-821PGL provides a gain factor of 1/2/4/8** and the **A-821PGH provides 1/10/100/1000.** The gain control register controls the gain of the A/D input signal. Bipolar/Unipolar will affect the gain factor.

It is important to select the correct gain-control-code according to Bipolar/Unipolar input.

NOTE : **If the gain control code is changed, the hardware needs to delay extra gain settling time.** The gain settling time is different for different gain control code. **The dos software driver does not control the gain settling time, so the user must delay the gain settling time if the gain is changed.**

A-821PGL GAIN CONTROL CODE TABLE

GAIN	Input Range	GAIN1	GAIN0	Settling Time
1	+/- 5 V	0	0	23 μ s
2	+/- 2.5 V	0	1	23 μ s
4	+/- 1.25 V	1	0	25 μ s
8	+/- 0.625 V	1	1	28 μ s

A-821PGH GAIN CONTROL CODE TABLE

GAIN	Input Range	GAIN1	GAIN0	Settling Time
1	+/- 5 V	0	0	23 μ s
10	+/- 0.5 V	0	1	28 μ s
100	+/- 0.05 V	1	0	140 μ s
1000	+/- 0.005 V	1	1	1300 μ s

2.4.7 A/D Multiplex Control Register

(WRITE) Base+A : A/D Multiplexer Control Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	D3	D2	D1	D0

A/D input channel selection data = 4 bits : D3...D0, D3=MSB, D0=LSB, X=don't care

Single-ended mode : D3..D0

Differential mode : D2..D0, D3=don't care

The A-821PGL/PGH provides 16 single-ended or 8 differential analog input signals. In single-ended mode, D3~D0 selects the active channel. In differential mode, D2~D0 selects the active channel and D3 will be "X" (don't care).

NOTE: The settling time of the multiplexer depends on the source resistance of input sources.

source resistance = about 0.1kOhm → settling time = about 3 μ s.

source resistance = about 1 kOhm → settling time = about 5 μ s.

source resistance = about 10 kOhm → settling time = about 10 μ s.

source resistance = about 100 kOhm → settling time = about 100 μ s.

Sec 2.4.6 gives information about how to delay the settling time.

2.4.8 A/D Mode Control Register

(WRITE) Base+B : A/D Mode Control Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	SI2	SI1	SI0	X	D2	D1	D0

X=don't care

Mode Select			Trigger Type		Transfer Type	
D2	D1	D0	Software Trig	Pacer Trig	Software	Interrupt
0	0	0	Select	X	Select	X
0	0	1	Select	X	Select	X
0	1	0	X	Select	X	X
1	1	0	X	Select	Select	Select

X=disable

SI2	SI1	SI0	IRQ Level
0	0	0	IRQ2
0	0	1	Not Used
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IIRQ5
1	1	0	IRQ6
1	1	1	IRQ7

The A/D conversion operation can be divided into 2 stages, **trigger stage and transfer stage**. The trigger stage will generate a trigger signal to the A/D converter and the transfer stage will transfer the result to the CPU.

The trigger method may be **Software trigger** or **Pacer trigger**. **The software trigger is very simple but cannot control the sampling rate precisely.** In software trigger mode, the program issues a software trigger command (sec 2.4.9) any time needed. Then the program will poll the A/D status bit until the busy bit is 0(sec 2.4.2).

The pacer trigger can control the sampling rate very precisely. So the converted data can be used to reconstruct the waveform of the analog input signal. In pacer trigger mode, the pacer timer (sec 2.6) will periodically generate trigger signals to the A/D converter. These converted data can be transfer to the CPU by polling or interrupt.

The software driver provides **polling or interrupt transfer**. The polling subroutine, A-822_AD_PollingVar() or A-822_AD_PollingArray(), sets the A/D mode control register to **0x01**. This control word means software trigger and polling transfer. The interrupt subroutine, A-822_AD_INT_START(...), sets the A/D mode control mode register to **0x06**. This control word means pacer trigger and interrupt transfer.

2.4.9 A/D Software Trigger Control Register

(WRITE) Base+C : A/D Software Trigger Control Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	X	X	X

X=don't care, XXXXXXXX=any 8 bits data is validate

The A/D converter can be triggered by software trigger or pacer trigger. Detailed information is given in sec. 2.4.8 and sec. 2.7. Writing any value to address BASE+C will generate a trigger pulse to A/D converter and initiate an A/D conversion operation. The address BASE+5 offers a busy bit to indicate an A/D conversion has been complete.

The software driver uses this control word to detect the A-821PGL/PGH hardware board. **The software initiates a software trigger and checks the busy bit.** If the busy bit cannot clear to zero in a fixed time, the software driver will return an error message. If there is an I/O BASE address setting error, the busy bit will not be cleared to zero. The software driver, **A-821_CheckAddress()**, uses this method to detect the correctness of the I/O BASE address setting

2.4.10 D/O Output Latch Register

(WRITE) Base+D : D/O Output Latch Low Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

(WRITE) Base+E : D/O Output Latch High Byte Data Format

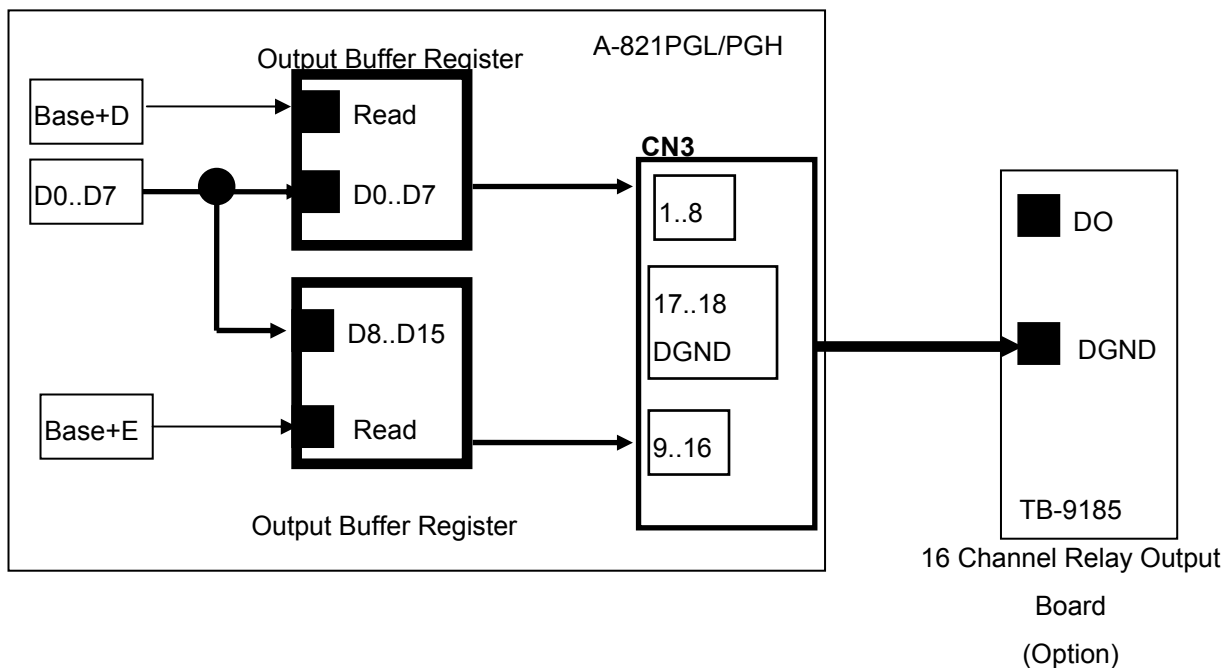
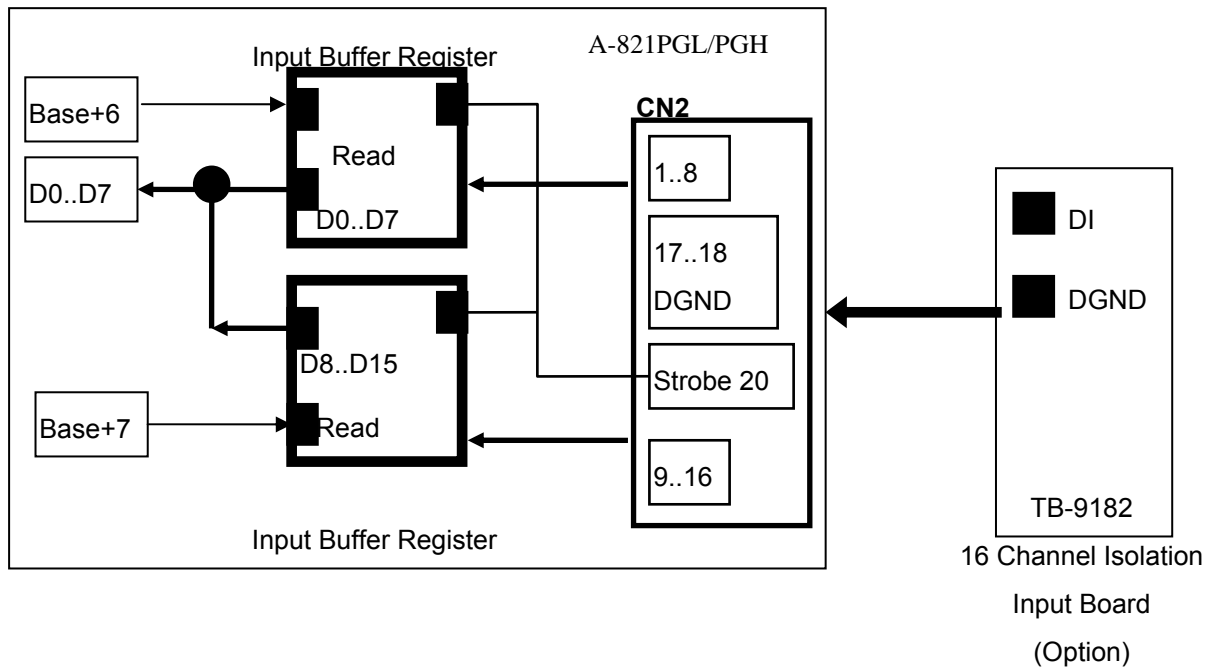
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D15	D14	D13	D12	D11	D10	D9	D8

D/O 16 bits output data : D15...D0, D15=MSB, D0=LSB

The A-821PGL/PGH provides 16 TTL compatible digital outputs. The low 8 bits are stored in address **BASE+D**. The high 8 bits are stored in address **BASE+E**

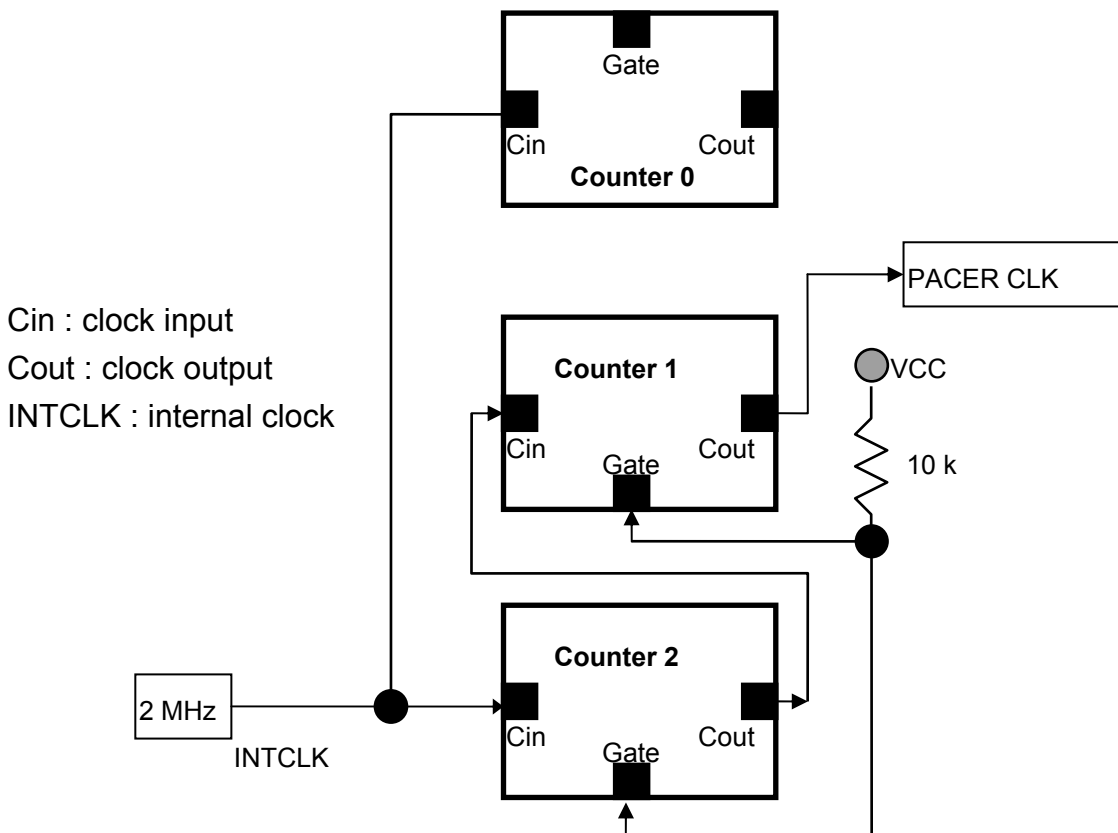
2.5 Digital I/O

The A-821PGL/PGH provides 16 digital input channels and 16 digital output channels. All levels are TTL compatible. The connections diagram and block diagram are given below:



2.6 8254 Timer/Counter

The 8254 Programmable timer/counter has 4 registers from Base+0 through Base+3. For detailed programming information about the 8254, please refer to Intel's "Microsystem Components Handbook". The block diagram is as below.



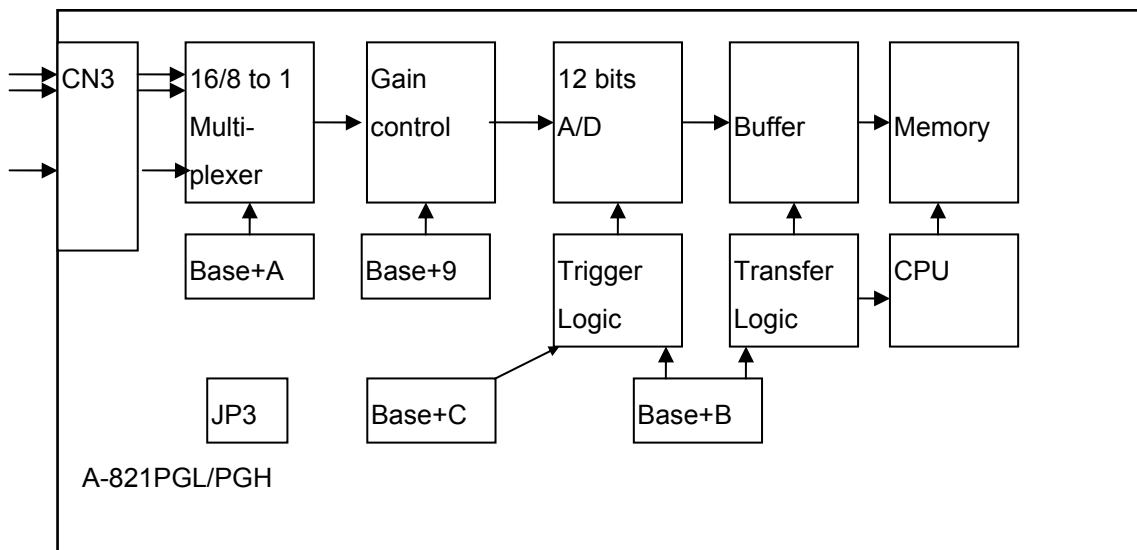
Counter1 and counter2 are both 16-bit counters. **Counter1 and counter2 are cascaded as a 32-bit timer.** This 32-bit timer is used as a **pacер timer**. Function of counter 0 is reserved.

2.7 A/D Conversion

This section explains how to use A/D conversions. The A/D conversion can be active **by software trigger or pacer trigger**. At the end of the A/D conversion, it is possible to transfer data by **polling and interrupt**. Before using the A/D conversion function, users should notice the following issues:

- * A/D data register, BASE+4/BASE+5, stores the A/D conversion data (**sec. 2.4.2**)
- * A/D gain control register, BASE+9, selects gain (**sec. 2.4.6**)
- * A/D multiplex control register, BASE+A, selects analog input (**sec. 2.4.7**)
- * A/D mode control register, BASE+B, selects trigger type and transfer type (**sec. 2.4.8**)
- * A/D software trigger control register, BASE+C (**sec. 2.4.9**)
- * JP3 selects single-ended or differential input (**sec. 2.3.3**)

The block diagram is given below:



2.7.1 A/D conversion flow

Next, the user must decide which A/D conversion mode will be used. The software driver supports **polling or interrupt mode**. The user can control the A/D conversion by polling mode very easily (sec. 2.4.9). It is recommended to use the software driver if using interrupt mode

The analog input signals come from CN1. These signals may be single-ended or differential type and must match with the setting of JP3.

The multiplexer can select 16 single-ended or 8 differential signals into the gain control module. The gain control module also needs settling time if the gain control code is changed. Because the dos software **doesn't manage the settling time, the user should delay enough settling time to accommodate for gain control code changes. (sec. 2.4.6)**

The output of the gain control module feeds into the A/D converter. **The A/D converter needs a trigger signal to start the A/D conversion cycle.** The A-821PGL/PGH supports **software trigger or pacer trigger mode.**

2.7.2 A/D Conversion Trigger Modes

The A-821PGL/PGH supports two trigger modes.

1 : Software Trigger :

Writes any value to A/D software trigger control register, BASE+C, will initiate an A/D conversion cycle. This mode is very simple but very difficult to control the sampling rate.

2 : Pacer Trigger Mode :

The block diagram of the pacer timer is shown in section 2.6. The pacer timer gives very precise sampling rates.

2.7.3 A/D Transfer Modes

A-821PGL/PGH supports two transfer modes.

Polling transfer :

This mode can be used with both trigger modes. Detailed information is given in section 2.4.8. The software scans A/D high byte data register, BASE+5, until BUSY_BIT=0. The low byte data is also ready in BASE+4.

Interrupt transfer :

This mode can be used with the pacer trigger. Detailed information is given in section 2.4.8. The user can set the IRQ level by using software (Base+B). A hardware interrupt signal is sent to the PC when an A/D conversion is completed.

2.7.4 Using software trigger and polling transfer

If the user needs to direct control the A/D converter without the A-821 software driver. It is recommended to use software trigger and polling transfer. The program steps are listed as below:

1. send 0x01 to A/D mode control register (software trigger + polling transfer)
(refer to Sec. 2.4.8)
2. send channel number to multiplexer control register **(refer to Sec. 2.4.7)**
3. send the gain control code value to gain control register **(refer to Sec 2.4.6)**
4. delay the settling time **(refer to Sec. 2.4.6 and Sec. 2.4.7)**
5. send any value to software trigger control register to generate a software trigger signal
(refer to Sec. 2.4.9)
6. scan the BUSY bit of the A/D high byte data until BUSY=0 **(refer to Sec. 2.4.2)**
7. read the 12 bits A/D data **(refer to Sec. 2.4.2)**
8. convert this 12 bits binary data to floating point value
(refer to "A-821 DOS Software Manual, Sec. 4.7 and Sec. 4.8)

2.8 D/A Conversion

The A-821PGL/PGH provides two 12-bit D/A converters. Before using the D/A conversion function, users should notice the following issues:

- * D/A output register, BASE+4/ BASE+5 (sec. 2.4.3)
- * JP1/JP2 select internal reference voltage -5 V/-10 V (sec. 2.3.1)

NOTE : The DA output latch registers are designed as “double buffer” structure.

The user must send the low byte data first, then send the high byte data to store the DA 12-bit digital data. If the user only sends the high byte data, then the low byte data will still be the previous value. Also, if the user sends high byte first then sends low byte, the low byte data of DA are still held in the previous one.

2.9 Analog Input Signal Connection

The A-821PGL/PGH can measure single-ended or differential type analog input signals. Some analog signals can be measured in both single-end and differential mode, but some can only be measured in either single-ended or differential mode. The user must decide which mode is suitable for measurement.

In general, there are 3 different analog signal connection methods as shown in Fig1 to Fig3. Fig1 is suitable for grounding source analog input signals. Fig2 can measure more channels than Fig1, but is only suitable for large analog input signals. Fig3 is suitable for thermocouple and Fig4 is suitable for floating source analog input signals.

Note : In Fig3, the maximum common mode voltage between the analog input source and the AGND is 70 V_{p-p}, so the user must make sure that the input signal is under specification first. If the common mode voltage is over 70 V_{p-p}, the input multiplexer will be damaged forever.

The simple way to select the input signal connection configuration is as below.

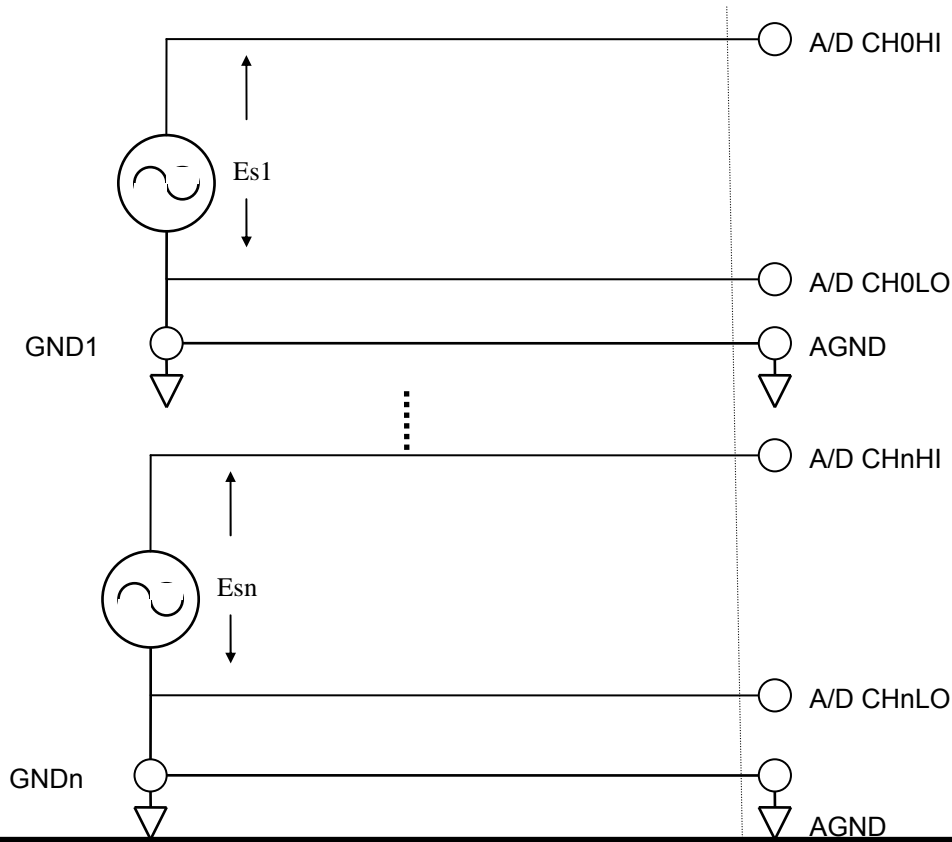
1. **Grounding source input signal** → **select Fig1**
2. **Thermocouple input signal** → **select Fig3**
3. **Floating source input signal** → **select Fig4**
4. **If V_{in} > 0.1 V and gain ≤ 10 (Low gain) and more channels are needed** → **select Fig2**

If the user is not able to determine the characteristics of the input signal, the test steps are given as below:

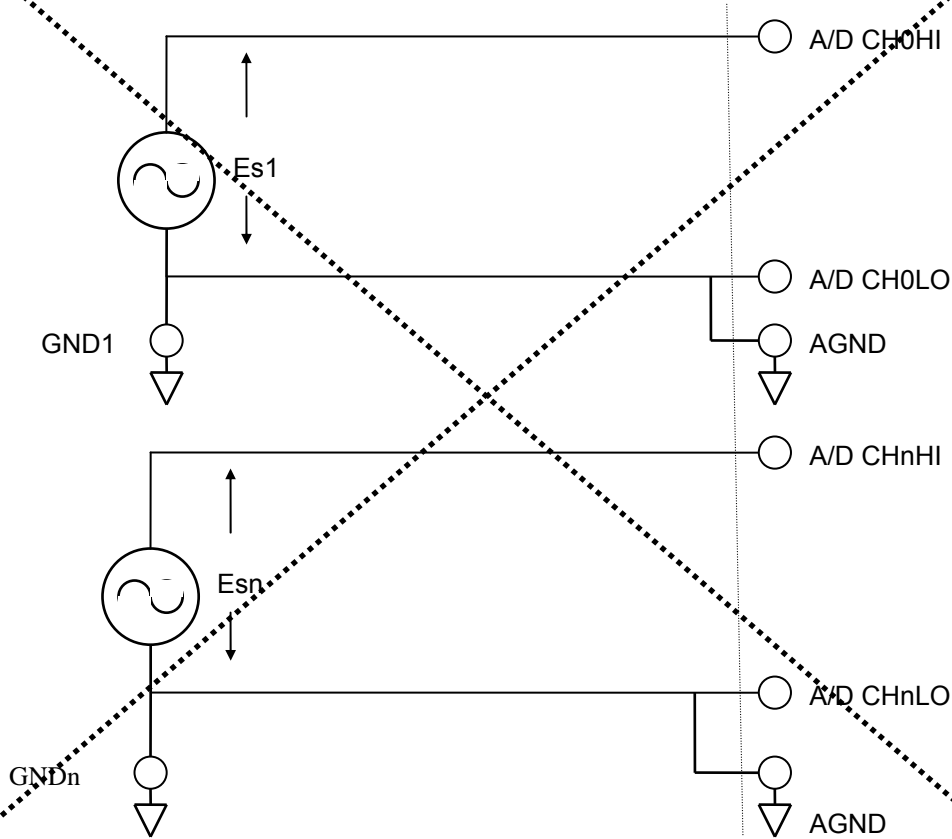
1. **Step1 : try Fig1 and record the measurement results**
2. **Step2 : try Fig4 and record the measurement results**
3. **Step3 : try Fig2 and record the measurement results**
4. **Compare the measurement results of step1, step2, step3 and select the best one**

1. FG1 : Connecting to grounding source input (Right way)

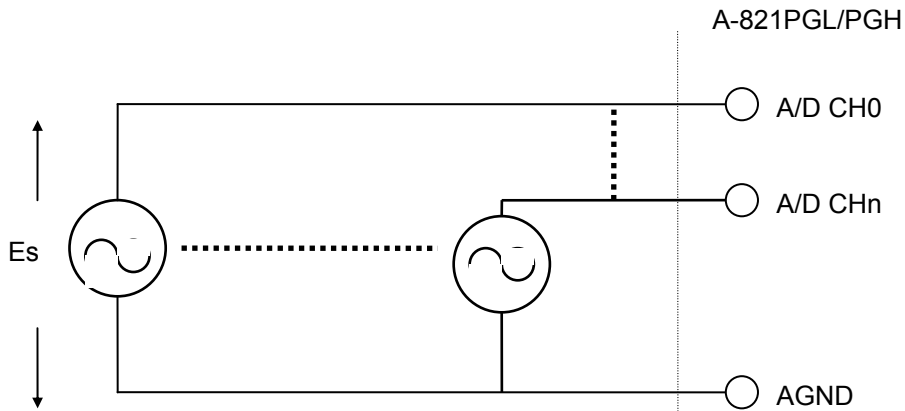
A-821PGL/PGH



FG1 : Wrong way

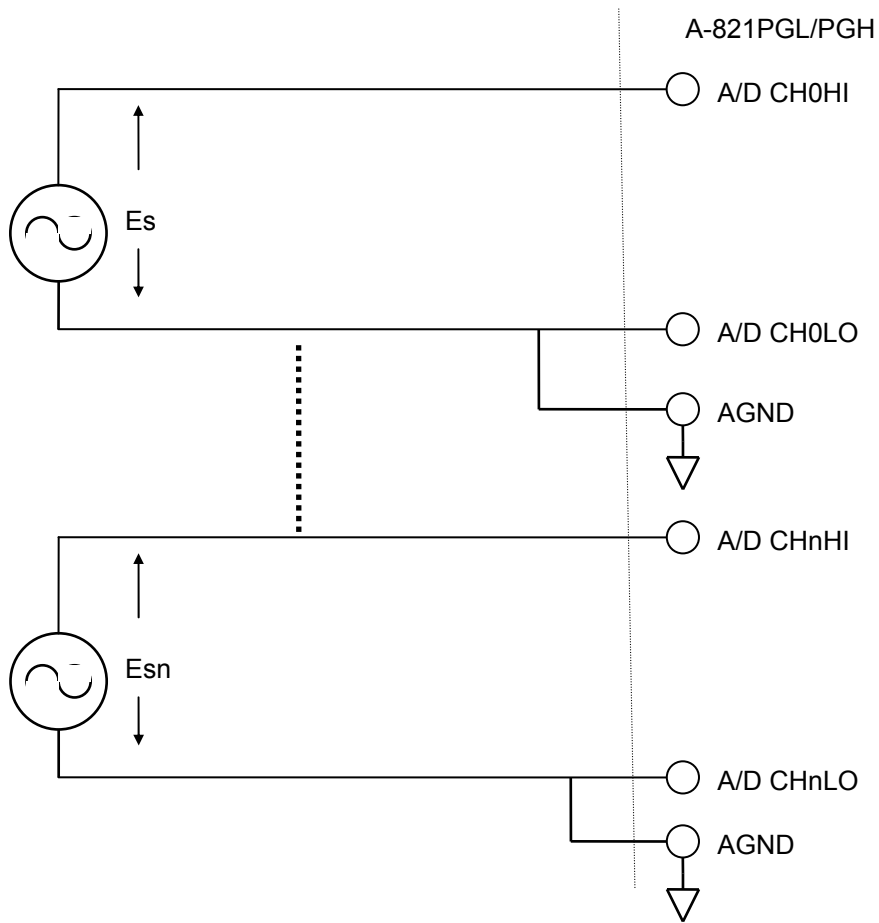


FG2 : Connecting to singled-ended input configuration



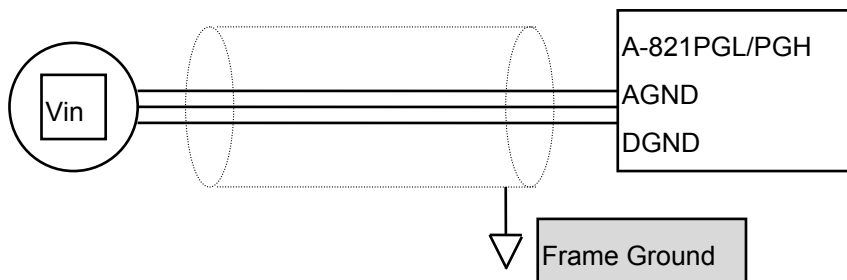
CAUTION : The maximum common mode voltage between the analog input source and the AGND is $70 V_{p-p}$, so the user must make sure that the input signal is under specification first. If the common mode voltage is over $70 V_{p-p}$, the input multiplexer will be damaged forever.

FG3 : connecting to floating source configuration



Signal Shielding

- * Signal shielding connections in Fig1 to Fig4 are all the same
- * Use single-point connection to **frame ground (not AGND or DGND)**



2.10 Using DB-8225 CJC Output

The DB-8225 daughter board with built-in CJC Circuitry, provided with the A-821PGL/PGH, produces 10 mV per Deg C With 0.0 Volts @ -273 Deg C. The A-821 should be protected from draughts and direct sunlight in order to accurately reflect room temperature.

CJC Calibration:

1. Connect the A-821PGL/PGH to DB-8215 CN1
2. Set the A-821PGL/PGH to Single-ended Mode
3. Set JP1 to 1-2 and JP2 to 2-3 (Single-ended mode)
4. Read the temperature from a digital thermometer placed near D1/D2
(See DB-8225 layout).
5. Read the A-821PGL/PGH analog input channel 0 (single-ended channel 0)
6. Adjust VR1 until a stable reading of 10 mV per deg C is attained.

For example, when the environment temperature is 24 deg C. the reading value of CJC will be 2.97 V

$$(273 \text{ deg c} + 24 \text{ deg c}) \times 10 \text{ mV/deg c} = 2.97 \text{ V}$$

You should use an A/D Channel for CJC calibration. AI0 is reserved for the CJC calibration used in single ended mode and CH0-HI & CH0-LO are reserved for differential mode. It is recommended to use differential mode if measuring thermocouple.

3 Connector

The A-821PGL/PGH provides three connectors: CN2 for 16 bits digital input, CN3 for 16 digital output and CN1 for analog input, analog output.

3.1 CN1/CN2/CN3 Pin Assignment

CN2 : Digital Input Connector Pin Assignment

Pin Number	Description	Pin Number	Description
1	Digital Input 0/TTL	2	Digital Input 1/TTL
3	Digital Input 2/TTL	4	Digital Input 3/TTL
5	Digital Input 4/TTL	6	Digital Input 5/TTL
7	Digital Input 6/TTL	8	Digital Input 7/TTL
9	Digital Input 8/TTL	10	Digital Input 9/TTL
11	Digital Input 10/TTL	12	Digital Input 11/TTL
13	Digital Input 12/TTL	14	Digital Input 13/TTL
15	Digital Input 14/TTL	16	Digital Input 15/TTL
17	PCB's GND output	18	PCB's GND output
19	PCB's +5 V output	20	STROBE

CN3 : Digital Output Connector Pin Assignment

Pin Number	Description	Pin Number	Description
1	Digital Output 0/TTL	2	Digital Output 1/TTL
3	Digital Output 2/TTL	4	Digital Output 3/TTL
5	Digital Output 4/TTL	6	Digital Output 5/TTL
7	Digital Output 6/TTL	8	Digital Output 7/TTL
9	Digital Output 8/TTL	10	Digital Output 9/TTL
11	Digital Output 10/TTL	12	Digital Output 11/TTL
13	Digital Output 12/TTL	14	Digital Output 13TTL
15	Digital Output 14/TTL	16	Digital Output 15/TTL
17	PCB's GND output	18	PCB's GND output
19	PCB's +5 V output	20	PCB's +12 V output

FOR SINGLE-ENDED SIGNALS

CN1 : Analog input/Analog output Connector Pin Assignment.

Pin Number	Description	Pin Number	Description
1	Analog Input 0/+	20	Analog Input 8/+
2	Analog Input 1/+	21	Analog Input 9/+
3	Analog Input 2/+	22	Analog Input 10/+
4	Analog Input 3/+	23	Analog Input 11/+
5	Analog Input 4/+	24	Analog Input 12/+
6	Analog Input 5/+	25	Analog Input 13/+
7	Analog Input 6/+	26	Analog Input 14/+
8	Analog Input 7/+	27	Analog Input 15/+
9	Analog GND	28	Analog GND
10	Analog GND	29	Analog GND
11	Not Used	30	D/A channel 0's analog voltage output
12	Not Used	31	Not Used
13	PCB's +12 V output	32	Not Used
14	Analog GND	33	Not Used
15	Digital GND	34	Not Used
16	Not Used	35	Not Used
17	Not Used	36	Not Used
18	Not Used	37	Not Used
19	PCB's +5 V output		

FOR DIFFERENTIAL SIGNALS

CN1 : Analog input/Analog output Connector Pin Assignment

Pin Number	Description	Pin Number	Description
1	Analog Input 0/+	20	Analog Input 0/-
2	Analog Input 1/+	21	Analog Input 1/-
3	Analog Input 2/+	22	Analog Input 2/-
4	Analog Input 3/+	23	Analog Input 3/-
5	Analog Input 4/+	24	Analog Input 4/-
6	Analog Input 5/+	25	Analog Input 5/-
7	Analog Input 6/+	26	Analog Input 6/-
8	Analog Input 7/+	27	Analog Input 7/-
9	Analog GND	28	Analog GND
10	Analog GND	29	Analog GND
11	Not used	30	D/A channel 0's analog voltage output
12	Not used	31	Not used
13	PCB's +12 V output	32	Not used
14	Analog GND	33	Not used
15	Digital GND	34	Not used
16	Not used	35	Not used
17	Not used	36	Not used
18	Not used	37	Not used
19	PCB's +5 V output	XXXXXXX	This pin not available

3.2 Daughter Board

The A-821PGL/PGH can be connected with many different daughter boards. The function of these daughter boards are described as follows.

3.2.1 DB-8225

The DB-8225 provides an **on-board CJC** (Cold Junction Compensation) circuit for thermocouple measurement and **terminal block** for easy signal connection and measurement. The CJC is connected to A/D channel_0. The A-821PGL/PGH can connect CN1 directly to DB-8225 through a 37-pin D-sub connector.

3.2.2 DB-37

The DB-37 is a **general purpose** 37-pin connector. This board directly connects to a 37-pin D-sub connector. It is suitable for easy signal connection and measurement.

3.2.3 DB-16P

The DB-16P (or 782 series) is a **16 channel isolated digital input** board. The A-821PGL/PGH provides 16 channel non-isolated TTL-compatible digital inputs from CN2. If connecting to DB-16P, the A-821PGL/PGH can provide 16 isolated digital input channels. Isolation can protect PC if abnormal input signal is occurred.

3.2.4 DB-16R

The DB-16R (or 785 series) provides **16-channel SPDT relay output**. The A-821PGL/PGH provides 16-channel TTL-compatible digital output from CN3. If connected to the DB-16R, the A-821PGL/PGH can provide 16-channel relay output to control power devices.

4. Calibration

The A-821PGL/PGH is calibrated to its best state of operation. For environments with large amount of vibration, recalibration is recommended. Before calibrating the A-821PGL/PGH, users should take care of the following issues:

- * One 6-digit multimeter
- * One stable voltage source (4.9988 V)
- * Diagnostic program : this program included in the delivered package will guide the user in further calibration.

4.1 Calibration VR Description

There are five VRs on the A-821PGL/PGH. Calibration needs to adjust all the VRs.

VR Num.	Description
VR1	D/A Gain adjustment
VR2	D/A Offset adjustment
VR3	A/D Offset adjustment
VR4	A/D Gain adjustment
VR5	A/D PGA adjustment (Programmable Gain Amplifier)

4.2 D/A Calibration Steps

1. Run A82xDIAG.EXE
2. Press "Right Arrow Key" to select "CALIBRATION" item
3. Select & Execute "A. D/A Offset " item
4. Connect D/A channel 0, pin 30 of CN1, to DVM
5. Adjust VR2 until DVM=0 V
6. Press "ESC Key"
7. Select & Execute "B. D/A REFERENCE" item
8. Adjust VR1 until DVM=4.9988V

4.3 A/D Calibration Steps

1. Run A-82XDIAG.EXE
2. Select "CARD TYPE" to A-821
3. Press "Right Arrow Key" to select "CALIBRATION" item
4. Press "Down Arrow Key" to select "C. A/D REFERENCE" item.
5. Press "Enter Key"
6. Input stable 4.9988 V to A/D channel 0, pin 1 of CN1
7. Adjust VR4 until A/D data shown in screen between 4094 to 4095
8. Press "ESC Key"
9. Select & Execute "D. A/D OFFSET" item
10. Input stable 0 V to A/D channel 0, pin1 of CN1
11. Adjust VR3 until A/D data shown in screen between 2048 to 2049
12. Press "ESC Key"
13. Repeat step_3 to step_11 until no need to adjust VR4,VR3
14. Select & Execute "E. PGA OFFSET" item
15. Input stable 0 V to A/D channel 0, pin 1 of CN1
16. Adjust VR5 until A/D data shown in screen between 2048 to 2049
17. Press "ESC Key"

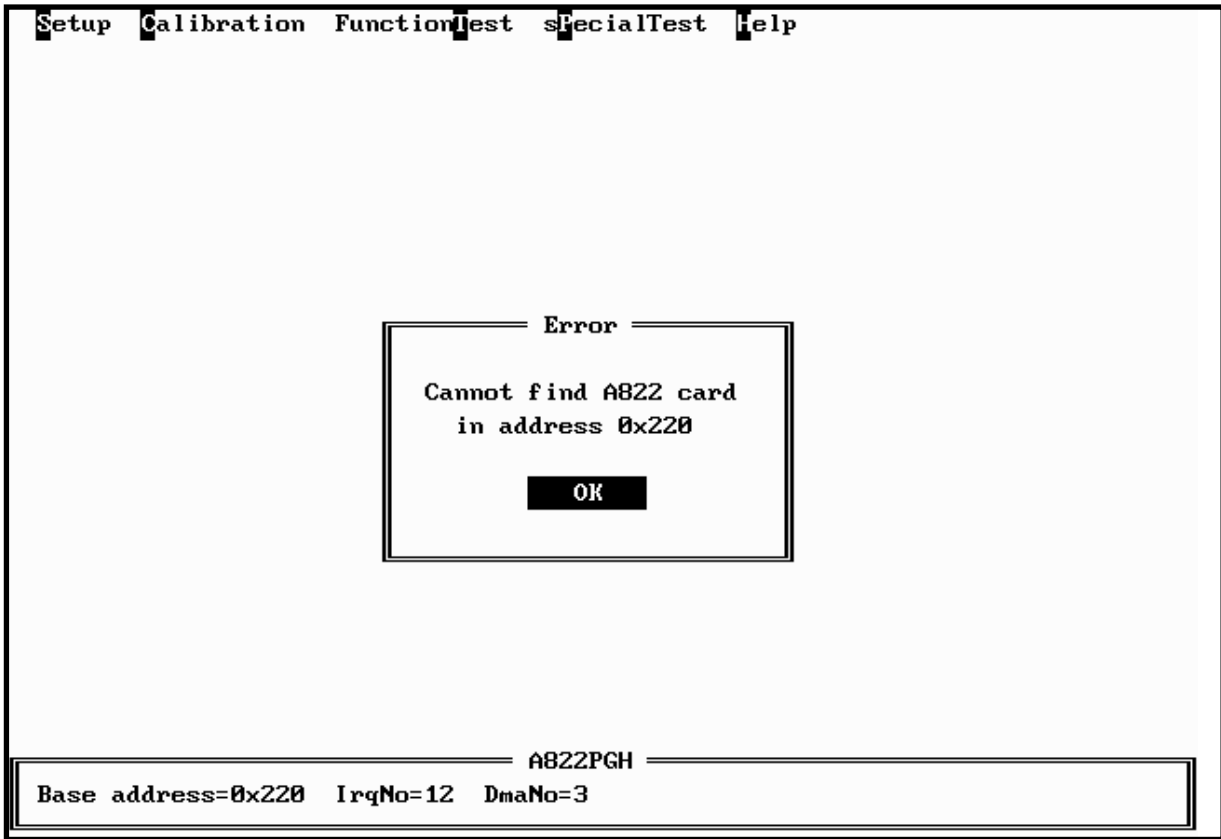
5 Diagnostic Utility

5.1 Introduction

The diagnostic utility, A-82XDIAG.EXE, is a menu-driven program which assists the user in a complete testing of the A-821PGL/PGH board. When in doubt regarding the operation of the A-821PGL/PGH board, run the diagnostic utility to check the functions of the board. To run the diagnostic utility, change to the subdirectory used in the installation process (C:\A-821 for example). Then type "A82XDIAG" <Enter> to start. The steps are shown as following:

```
C:\>CD A-822 <Enter>
C:\A-821>CD DIAG <Enter>
C:\A-821\DIAG>A-821DIAG <Enter>
```

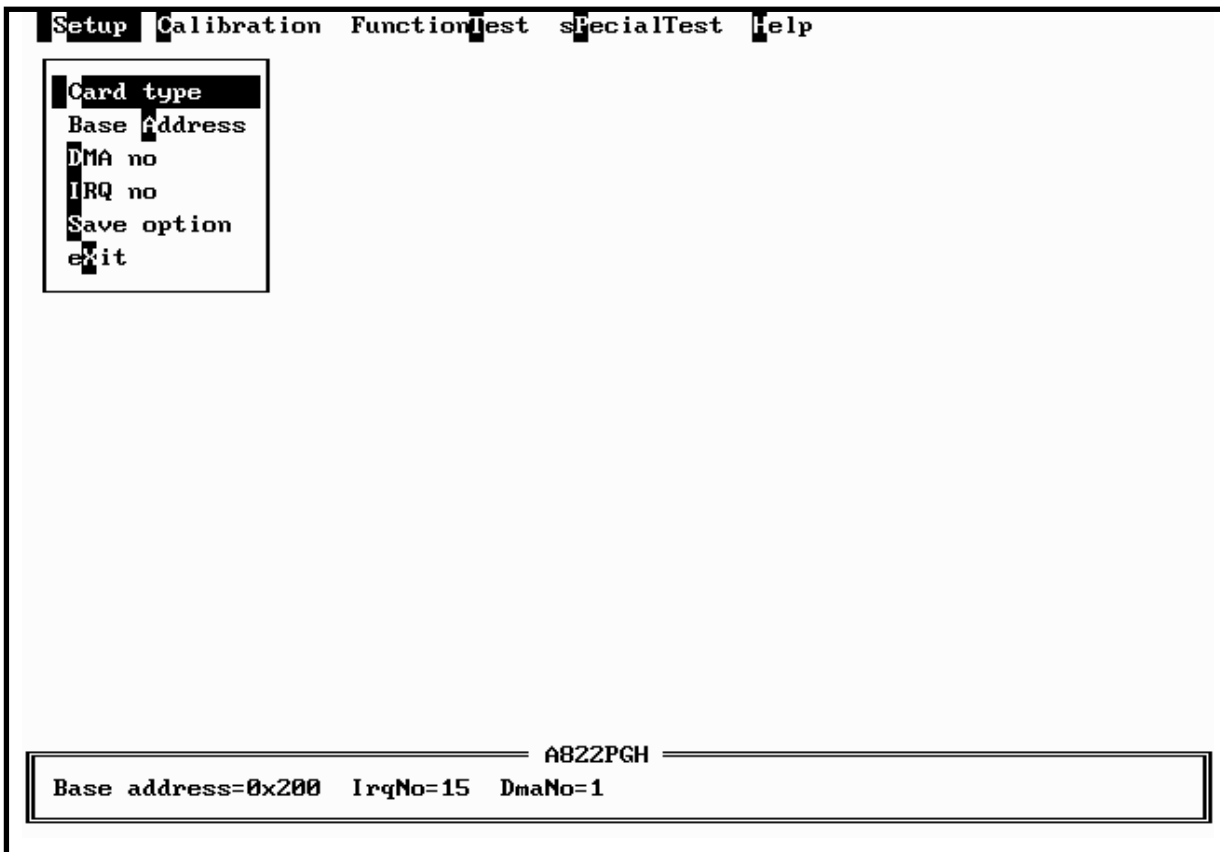
A configuration file, named A-82x.CFG, is associated with the A-82XDIAG.EXE. The configuration of the A-821PGL/PGH board is recorded in this file. The information includes the I/O base address, interrupt number and DMA channel number used by the A-821PGL/PGH. While the A-82XDIAG is running, if you make some adjustments, the changes will not be saved automatically. Therefore, the user must select the save function to save the changes. When A-82XDIAG.EXE starts up, it will automatically check if the jumper setting of the I/O base address is identical to the value stored in the configuration file. If the address is not identical, an error message will appear to warn you. The screen is shown as below.



Although you can continue by pressing any key, it is recommended to correct this situation by setting the proper jumper setting. Because many operations occur in the A-82XDIAG, the I/O base address is check first. And if the error occurs, it doesn't work.

5.2 Running Diagnostic Utility

The initialization screen of the A-82XDIAG is shown as below. As you can see, there are five items on the main menu in the initialization screen. They are Setup, Calibration, FunctionTest, sPecialTest and Help. Use the Left or Right key to select the items on the main menu. An item that is highlighted means it is selected, and some menu items are associated with it. Use the Up or Down key to select the sub items, those items will also be highlighted. Alternately, the user can press the command key to highlight the menu item. A command key in a menu item is the character which is highlighted. To proceed with a function associated the highlighted menu item, just press <Enter>. And press <Esc> to abort the current function.



5.2.1 Setup

“Setup” allows users to setup the board configuration. There are six functions in this item, Card type, Base Address, DMA no, IRQ no, Save option, eXit.

Card type : <Up/Down> key to select A-821PGL/PGH, <Enter> key to select

Base Address : <Up/Down> key to select base address, <Enter> key to select

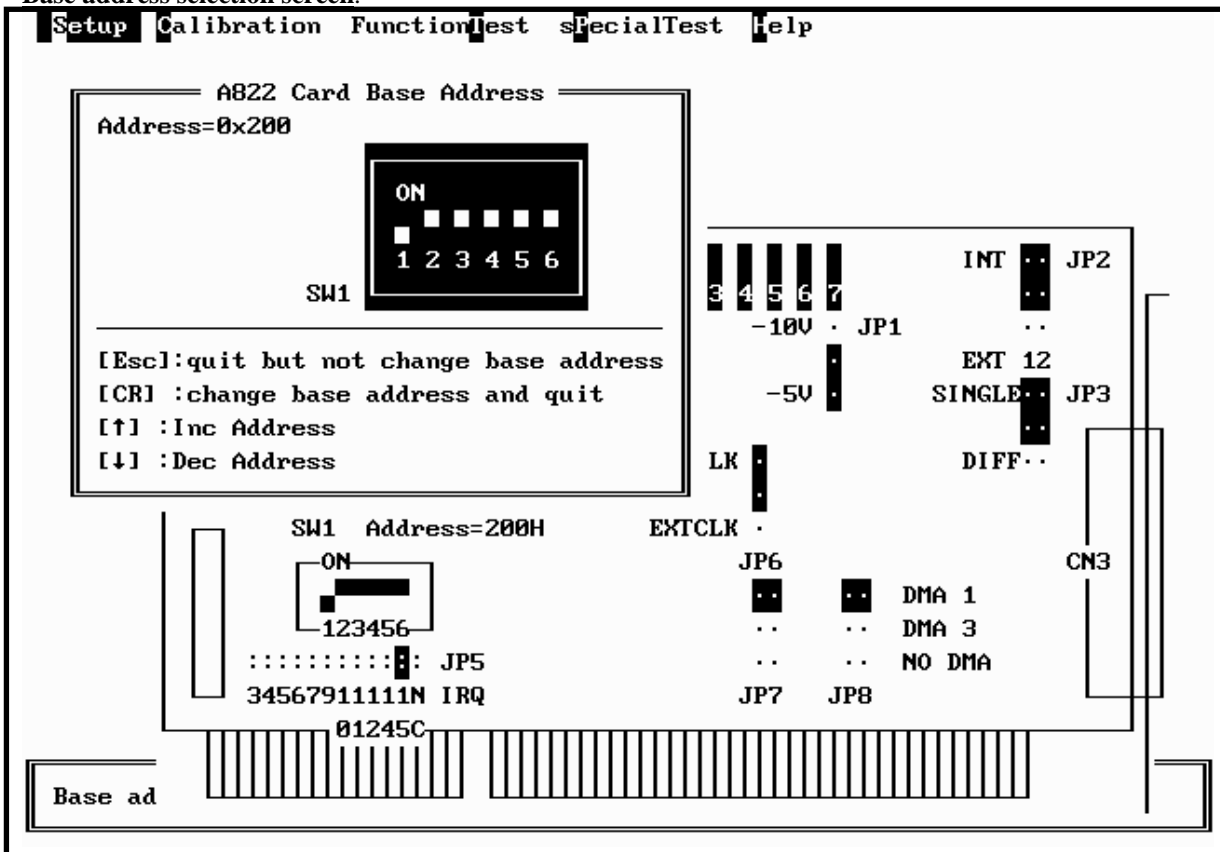
DMA no : <Up/Down> key to select DMA no, <Enter> key to select

IRQ no : <Left/Right> key to select IRQ no, <Enter> key to select

Save option : <Left/Right> key to select yes/no, <Enter> key to select

eXit : <Left/Right> key to select yes/no, <Enter> key to select

Base address selection screen.



DMA no and IRQ no selection screen

Setup Calibration FunctionTest SpecialTest Help

AB22 Card DMA No.

DMA=1 JP7 JP8

DMA1

DMA3

NODMA

[Esc]:quit but not change DMA No.
 [CR] :change DMA No. and quit
 [↑][↓] : Change setting

EXTTRG

CN2

SW1 Address=200H

ON

123456

.....: JP5

34567911111N IRQ

01245C

1 2 3 4 5 6 7

1 -10V · JP1

2 -5V ·

INTCLK ·

EXTCLK ·

JP6 DMA 1

 DMA 3

 NO DMA

JP7 JP8

INT JP2

..

EXT 12

SINGLE JP3

..

DIFF ..

CN3

Base ad

Setup Calibration FunctionTest SpecialTest Help

AB22 Card IRQ No.

IRQ=15

.....

.....

3 4 5 6 7 9 1 1 1 1 1 NC

0 1 2 4 5

[Esc]:quit but not change IRQ No.
 [CR] :change IRQ No. and quit
 [→] :Inc IRQ No.
 [←] :Dec IRQ No.

SW1 Address=200H

ON

123456

.....: JP5

34567911111N IRQ

01245C

1 2 3 4 5 6 7

1 -10V · JP1

2 -5V ·

INTCLK ·

EXTCLK ·

JP6 DMA 1

 DMA 3

 NO DMA

JP7 JP8

INT JP2

..

EXT 12

SINGLE JP3

..

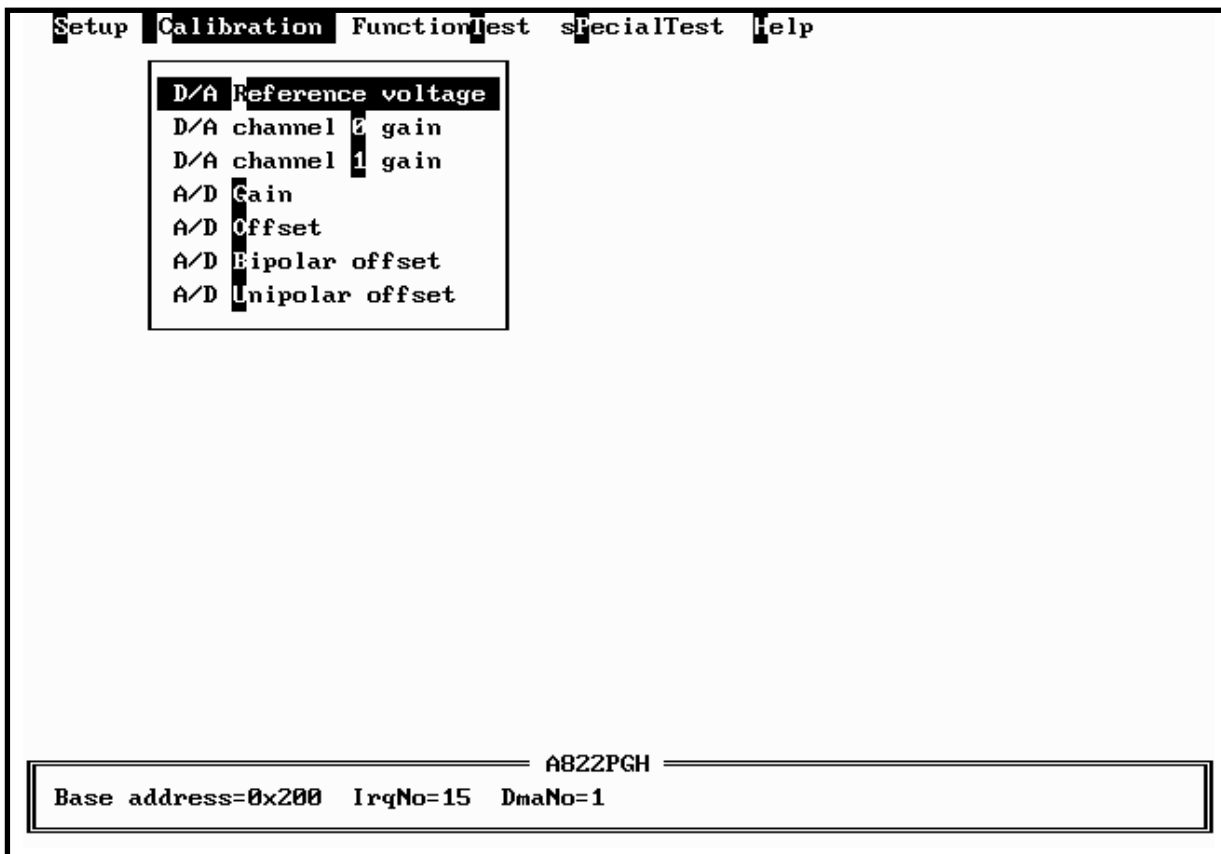
DIFF ..

CN3

Base ad

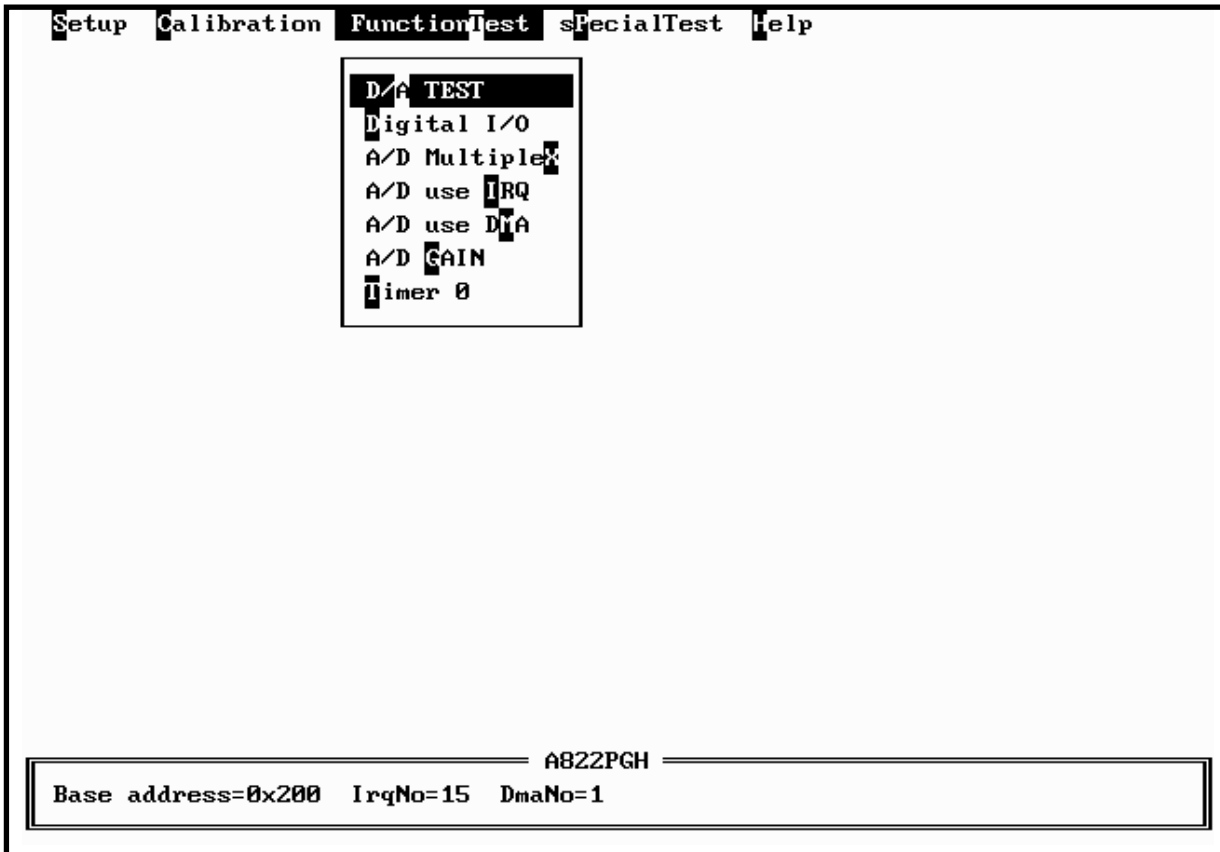
5.2.2 CALIBRATION

The "CALIBRATION" contains ten menu items: those are, D/A Reference voltage, D/A Channel 0 gain, D/A channel 1 gain, A/D Gain, A/D Offset, A/D Bipolar Offset, A/D Unipolar Offset. These items are concerning the calibration of the A-821PGL/PGH. In CALIBRATION main menu, a graphic presentation of the A-821PGL/PGH board's layout is shown. The calibration will become a visual process in order to reduce user's effort. To keep the optimal performance and correct precision for the board, it is useful to calibrate the board after working for a long time period. There are seven VRs that need to be tuned in the calibration process. When you highlight one of the first seven menu items, the associated VR begins blinking. And a message window will appear to direct the user how to tune the VRs. The main menu screen is shown as below.



5.2.3 FUNCTION TEST

The FUNCTION TEST main menu contains seven menu items: those are D/A TEST, Digital I/O, A/D MULTIPLEX, A/D use IRQ, A/D use DMA, A/D GAIN, Timer 0. The main menu is shown as below.



If selecting “D/A TEST” item, the screen is shown as below.

<D/A TEST > test screen

```
Setup Calibration FunctionTest SpecialTest Help

          DA Test
-----
Test count=2
  DA channel 1      DA channel 2
-----
0333H --> 1.000V   0333H --> 1.000V
-----
[p]:pause  [Esc]:quit
[↑]:Inc delay [↓]:Dec delay  delay= 400

          A822PGH
-----
Base address=0x200  IrqNo=15  DmaNo=1
```

- * assume D/A output range 0 ~ 5 V
- * send D/A output to both channels simultaneously
- * press <p> pause screen, press <p> again release screen
- * press <Up> key to increase screen delay
- * press <Down > key to delay screen delay
- * press <ESC> key to quit

<Digital I/O> test screen

```
Setup Calibration FunctionTest SpecialTest Help

Digital I/O TEST
Test count=154993
DO      DI      Test count=154993
Hex     Binary  Hex     Binary  Status
-----
[5D70]0101110101110000 [5D70]0101110101110000 OK.
[5D69]0101110101101001 [5D69]0101110101101001 OK.
[5D6A]0101110101101010 [5D6A]0101110101101010 OK.
[5D6B]0101110101101011 [5D6B]0101110101101011 OK.
[5D6C]0101110101101100 [5D6C]0101110101101100 OK.
[5D6D]0101110101101101 [5D6D]0101110101101101 OK.
[5D6E]0101110101101110 [5D6E]0101110101101110 OK.
[5D6F]0101110101101111 [5D6F]0101110101101111 OK.

Please use 20 pin flat cable connect CN1<->CN2 D= 0
[p]:pause [Esc]:quit [↑]:Inc delay [↓]:Dec delay

A822PGH
Base address=0x200 IrqNo=15 DmaNo=1
```

- * assume CN1 is direct connected to CN2
- * a 16 bits up counter is send to 16-channel DO
- * 16-channel DO direct connected to 16 channel DI
- * 16-channel DI is readback and show in screen
- * DO == DI → show OK in screen
- * DO != DI → show Error in screen
- * press <p> pause screen, press <p> again release screen
- * press <Up> key to increase screen delay
- * press <Down > key to reduce screen delay
- * press <ESC> key to quit

<A/D Multiplexer> test screen

Setup	Calibration	Function	Test	SpecialTest	Help
AD TEST [Polling]					
Test count=1515					
Channel Value					

0 4.795V					
1 3.972V					
2 3.967V					
3 3.301V					
4 4.009V					
5 3.262V					
6 2.651V					
7 1.948V					
8 1.274V					
9 0.925V					
10 0.674V					
11 0.439V					
12 0.356V					
13 0.049V					
14 -0.195V					
15 -0.459V					

A822PGH					
Base address=0x200 IrqNo=15 DmaNo=1					

- * assume 16-channel single-ended, bipolar, gain=1, analog input signals
- * input range from -5 V ~ +5 V
- * continue scanning between 16 channels
- * press <ESC> key to quit

<A/D use IRQ> test screen

```
Setup Calibration Function Test SpecialTest Help
----- AD TEST [Interrupt] -----
Test count=2
Channel= 0                      C1=10 C2=14 [ 14.3K Hz]
Read AD number= 999/1000      Max= 4.958 Min= 4.934 Average= 4.942
-----
[000]: 4.939 [020]: 4.939 [040]: 4.949 [060]: 4.946 [080]: 4.941
[100]: 4.937 [120]: 4.939 [140]: 4.949 [160]: 4.951 [180]: 4.941
[200]: 4.944 [220]: 4.939 [240]: 4.939 [260]: 4.944 [280]: 4.944
[300]: 4.941 [320]: 4.941 [340]: 4.941 [360]: 4.941 [380]: 4.951
[400]: 4.944 [420]: 4.939 [440]: 4.939 [460]: 4.944 [480]: 4.941
[500]: 4.941 [520]: 4.939 [540]: 4.939 [560]: 4.944 [580]: 4.941
[600]: 4.941 [620]: 4.941 [640]: 4.941 [660]: 4.941 [680]: 4.946
[700]: 4.946 [720]: 4.941 [740]: 4.941 [760]: 4.941 [780]: 4.939
[800]: 4.939 [820]: 4.937 [840]: 4.939 [860]: 4.941 [880]: 4.941
[900]: 4.941 [920]: 4.939 [940]: 4.941 [960]: 4.941 [980]: 4.951
-----
[p]:pause [Esc]:quit
[PageUp]:Inc channel [PageDn]:Dec channel
[↑]:Inc C1 [↓]:Dec C1 [←]:Inc C2 [→]:Dec C2
-----
A822PGH
-----
Base address=0x200 IrqNo=15 DmaNo=1
```

- * assume single-ended, bipolar, gain=1
- * use <PgUp> key to select the next channel
- * use <PgDn> key to select the previous channel
- * use <Up>/<Down> key to adjust C1
- * use <Left>/<Right> key to adjust C2
- * sampling rate = pacer timer rate = $2000/(C1 \cdot C2)$ K
- * use <p> key to pause screen, use next <p> key to release screen
- * use <ESC> to quit
- * A/D mode control register=0x06 → select pacer trigger and use interrupt transfer
- * one cycle sample 1000 A/D data continue
- * minimal/maximal/average value shown in screen

<A/D use DMA> test screen

```
Setup Calibration FunctionTest SpecialTest Help
----- AD TEST [Interrupt] -----
Test count=2
Channel= 0                               C1=10 C2=14 [ 14.3K Hz]
Read AD number= 999/1000                 Max= 4.958 Min= 4.934 Average= 4.942
-----
[000]: 4.939 [020]: 4.939 [040]: 4.949 [060]: 4.946 [080]: 4.941
[100]: 4.937 [120]: 4.939 [140]: 4.949 [160]: 4.951 [180]: 4.941
[200]: 4.944 [220]: 4.939 [240]: 4.939 [260]: 4.944 [280]: 4.944
[300]: 4.941 [320]: 4.941 [340]: 4.941 [360]: 4.941 [380]: 4.951
[400]: 4.944 [420]: 4.939 [440]: 4.939 [460]: 4.944 [480]: 4.941
[500]: 4.941 [520]: 4.939 [540]: 4.939 [560]: 4.944 [580]: 4.941
[600]: 4.941 [620]: 4.941 [640]: 4.941 [660]: 4.941 [680]: 4.946
[700]: 4.946 [720]: 4.941 [740]: 4.941 [760]: 4.941 [780]: 4.939
[800]: 4.939 [820]: 4.937 [840]: 4.939 [860]: 4.941 [880]: 4.941
[900]: 4.941 [920]: 4.939 [940]: 4.941 [960]: 4.941 [980]: 4.951
-----
[p]:pause [Esc]:quit
[PageUp]:Inc channel [PageDn]:Dec channel
[↑]:Inc C1 [↓]:Dec C1 [←]:Inc C2 [→]:Dec C2
-----
A822PGH
-----
Base address=0x200 IrqNo=15 DmaNo=1
```

- * assume single-ended, bipolar, gain=1
- * use <PgUp> key to select the next channel
- * use <PgDn> key to select the previous channel
- * use <Up>/<Down> key to adjust C1
- * use <Left>/<Right> key to adjust C2
- * sampling rate = pacer timer rate = $2000/(C1 \cdot C2)$ K
- * use <p> key to pause screen, use next <p> key to release screen
- * use <ESC> to quit
- * A/D mode control register=0x02 → select pacer trigger and use DMA transfer
- * one cycle sample 1000 A/D data continue
- * minimal/maximal/average value shown in screen

<DA GAIN> test screen

```
Setup Calibration FunctionTest SpecialTest Help

===== A/D Gain Test =====
GainMode=A822_BI_1                      Count=684
-----
A/D ch0=0x0BFF( 2.498)                   D/A ch0=0x0800( 2.500)
-----
Please connect CN3 pin 1 to CN3 pin 30
              (A/D 0)             (D/A 0)
[Esc]:quit  [↑][↓]:Change Gain
             [←][→]:Change D/A value

===== A822PGH =====
Base address=0x200  IrqNo=15  DmaNo=1
```

- * assume single-ended, bipolar, gain=1, A/D channel 0 connect to D/A channel 0
- * use <Up>/<Down> key to adjust gain control code
- * use <Left>/<Right> key to adjust D/A output value
- * use software trigger and polling transfer mode
- * press <ESC> key to quit

<Timer 0> test screen

```
Setup Calibration FunctionTest SpecialTest Help

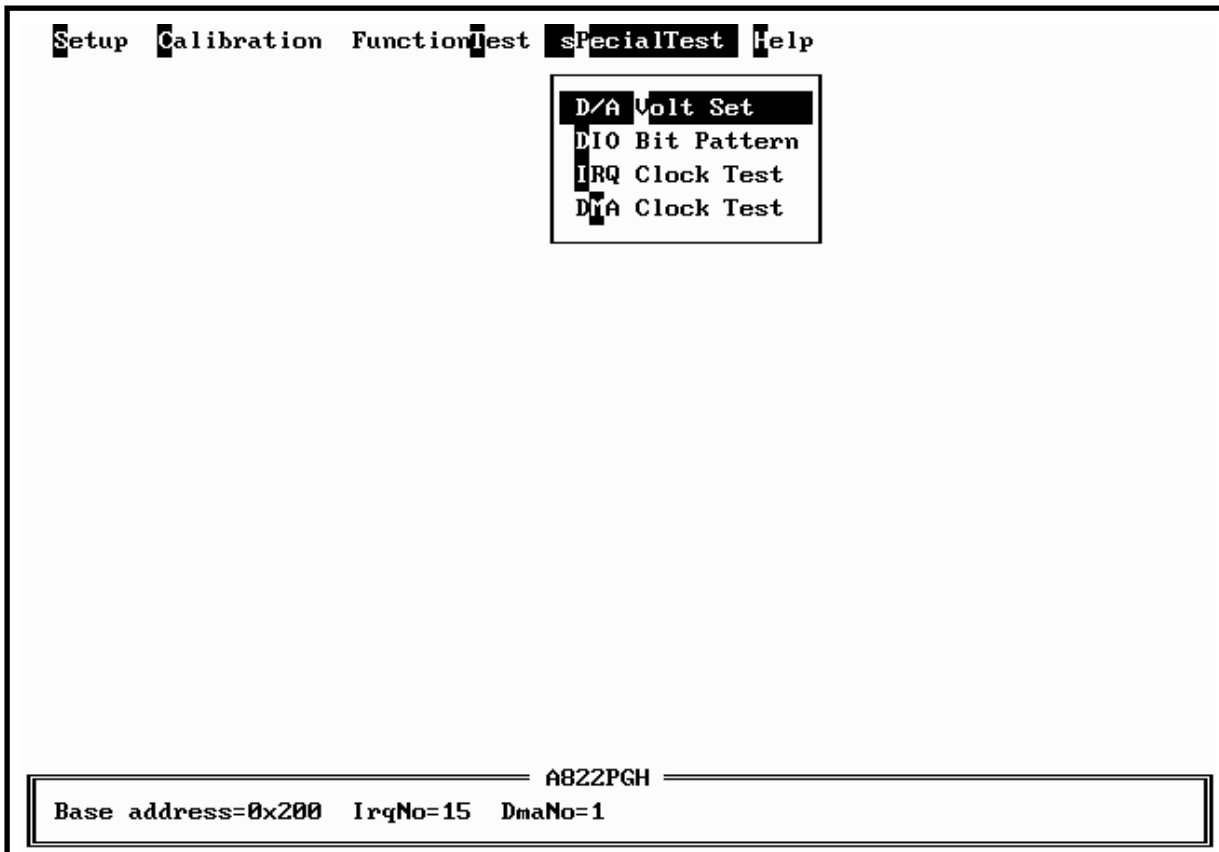
===== Timer 0 Test =====
Timer Mode=3
-----
Value=6C1C
-----
If value is not constant --> Timer is OK.
(CN3 pin 16 : high->low->high->low->... )
[Esc]:quit

===== A822PGH =====
Base address=0x200 IrqNo=15 DmaNo=1
```

- * assume JP6 select internal 2 M clock
- * If the counter0 is normal, the value will increment automatically. If the value is a fixed value, the counter0

5.2.4 SPECIAL TEST

The SPECIAL TEST main menu contains four menu items: those are D/A Volt Set, DIO Bit Pattern, IRQ Clock Test and DMA Clock Test. These functions are reserved for factory testing.



5.2.5 Help

The Help menu will show the software version as below.

